



Atty. Dkt. No. 039153-0693 (H1718)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Xiang et al.

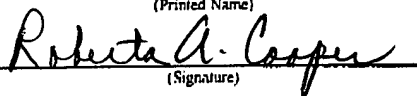
Title: SHALLOW TRENCH
ISOLATION PROCESS AND
STRUCTURE WITH MINIMIZED
STRAINED SILICON
CONSUMPTION

Appl. No.: 10/755,602

Filing Date: 01/12/2004

Examiner: Jack Chen

Art Unit: 2813

CERTIFICATE OF EXPRESS MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
EV 904367259 US	08/04/06
(Express Mail Label Number)	(Date of Deposit)
Roberta A. Cooper	
(Printed Name)	
	
(Signature)	

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

We, Qi Xiang, James N. Pan, and Jung-Suk Goo, state and declare that:

1. Each of us is an inventor of at least one of the claims currently pending in U.S. Patent Application No. 10/755,602 (hereinafter "the '602 application").
2. We understand that in an Office Action dated April 6, 2006, Claims certain of these claims were rejected as being unpatentable based in part on the use of U.S. Patent No. 6,878,606 to Ohnishi et al., entitled "FABRICATION METHOD AND DEVICE STRUCTURE OF SHALLOW TRENCH INSULATION FOR SILICON WAFER CONTAINING SILICON-GERMANIUM" (hereinafter "Ohnishi et al.").
3. We understand based on the information provided on the front page of Ohnishi et al. that Ohnishi et al. has a U.S. filing date of May 28, 2003.
4. At least by November 11, 2002, we conceived in the United States the ideas set forth in the pending claims of the '602 application. Such conception is evidenced by the attached invention disclosure form pertaining to the subject matter of the present application, and which is dated November 11, 2002 and signed by inventor Qi Xiang.

5. After conceiving the ideas set forth in the pending claims of the '602 application, we engaged in due diligence from prior to the May 28, 2003 filing date of Ohnishi et al. until the filing of the '602 application on January 12, 2004.
6. We believe that the individuals involved in the conception, preparation, and filing of the '602 application engaged in reasonable due diligence from prior to the May 28, 2003 filing date of Ohnishi et al. until the time of the filing date of the '602 application on January 12, 2004.
7. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

Date: _____

By: _____

Qi Xiang

Date: 7 / 31 / 06

By: James N Pan

James N. Pan

Date: _____

By: _____

Jung-Suk Goo



Atty. Dkt. No. 039153-0693 (H1718)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Xiang et al.

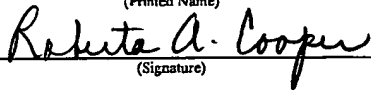
Title: SHALLOW TRENCH
ISOLATION PROCESS AND
STRUCTURE WITH MINIMIZED
STRAINED SILICON
CONSUMPTION

Appl. No.: 10/755,602

Filing Date: 01/12/2004

Examiner: Jack Chen

Art Unit: 2813

CERTIFICATE OF EXPRESS MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
EV 904367259 US	08/04/06
(Express Mail Label Number)	(Date of Deposit)
Roberta A. Cooper	
(Printed Name)	
	
(Signature)	

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

We, Qi Xiang, James N. Pan, and Jung-Suk Goo, state and declare that:

1. Each of us is an inventor of at least one of the claims currently pending in U.S. Patent Application No. 10/755,602 (hereinafter "the '602 application").
2. We understand that in an Office Action dated April 6, 2006, Claims certain of these claims were rejected as being unpatentable based in part on the use of U.S. Patent No. 6,878,606 to Ohnishi et al., entitled "FABRICATION METHOD AND DEVICE STRUCTURE OF SHALLOW TRENCH INSULATION FOR SILICON WAFER CONTAINING SILICON-GERMANTUM" (hereinafter "Ohnishi et al.").
3. We understand based on the information provided on the front page of Ohnishi et al. that Ohnishi et al. has a U.S. filing date of May 28, 2003.
4. At least by November 11, 2002, we conceived in the United States the ideas set forth in the pending claims of the '602 application. Such conception is evidenced by the attached invention disclosure form pertaining to the subject matter of the present application, and which is dated November 11, 2002 and signed by inventor Qi Xiang.

5. After conceiving the ideas set forth in the pending claims of the '602 application, we engaged in due diligence from prior to the May 28, 2003 filing date of Ohnishi et al. until the filing of the '602 application on January 12, 2004.
6. We believe that the individuals involved in the conception, preparation, and filing of the '602 application engaged in reasonable due diligence from prior to the May 28, 2003 filing date of Ohnishi et al. until the time of the filing date of the '602 application on January 12, 2004.
7. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

Date: _____

By: _____
Qi Xiang

Date: _____

By: _____
James N. Pan

Date: 7/3/2006


By: 
Jung-Suk Goo



EXHIBIT A

1-1

PRIORITY CODE	
A <input checked="" type="checkbox"/>	B <input type="checkbox"/>
C <input type="checkbox"/>	D <input type="checkbox"/>

(51)

MONDAY, NOVEMBER 11, 2002

TDG STRAINED SILICON ON INSULATOR (SSOI) PATENT HARVESTING

Technical Leader: Qi Xiang

AMD INVENTION DISCLOSURETLD ID# H 1718

Rec'd date _____

California & Asia: x44760, return to MS68;

Texas: x55964 return to MS562;

Dresden & Europe: x83401 Silke Kretzschmar at MS E21-PP.

This invention applies to: Project: ☐, Product: ☐, Process: ☐, Technology ☐, Other ☐,
IMPORTANT Please identify any potential use: _____

List 2 to 5 key search words related to the invention: _____

Working title of invention: SSOI CMOS with High Quality STI and Minimized S-Si Consumption

INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE (1A)

Inventor's signature: _____ date: _____

Inventor's printed full name: QI XIANG Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone() _____

AMD email address: _____ AMD office FAX() _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

Co-Inventor's signature : _____ date : _____

Co-Inventor's printed full name: _____ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone() _____

AMD email address: _____ AMD office FAX() _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

Co-Inventor's signature : _____ date : _____

Co-Inventor's printed full name: _____ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone() _____

AMD email address: _____ AMD office FAX() _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

Co-Inventor's signature : _____ date : _____

Co-Inventor's printed full name: _____ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone() _____

AMD email address: _____ AMD office FAX() _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

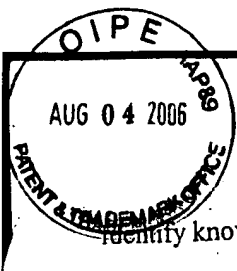
HARVESTING LAW FIRM/ATTORNEYS: FOLEY & LARDNER

Joe Ziebert & Ron Coslick

State total number of inventors here: _____. If there are more than four inventors, insert duplicate page 1.

Witness 1 initial: _____ Witness 2 initial: _____

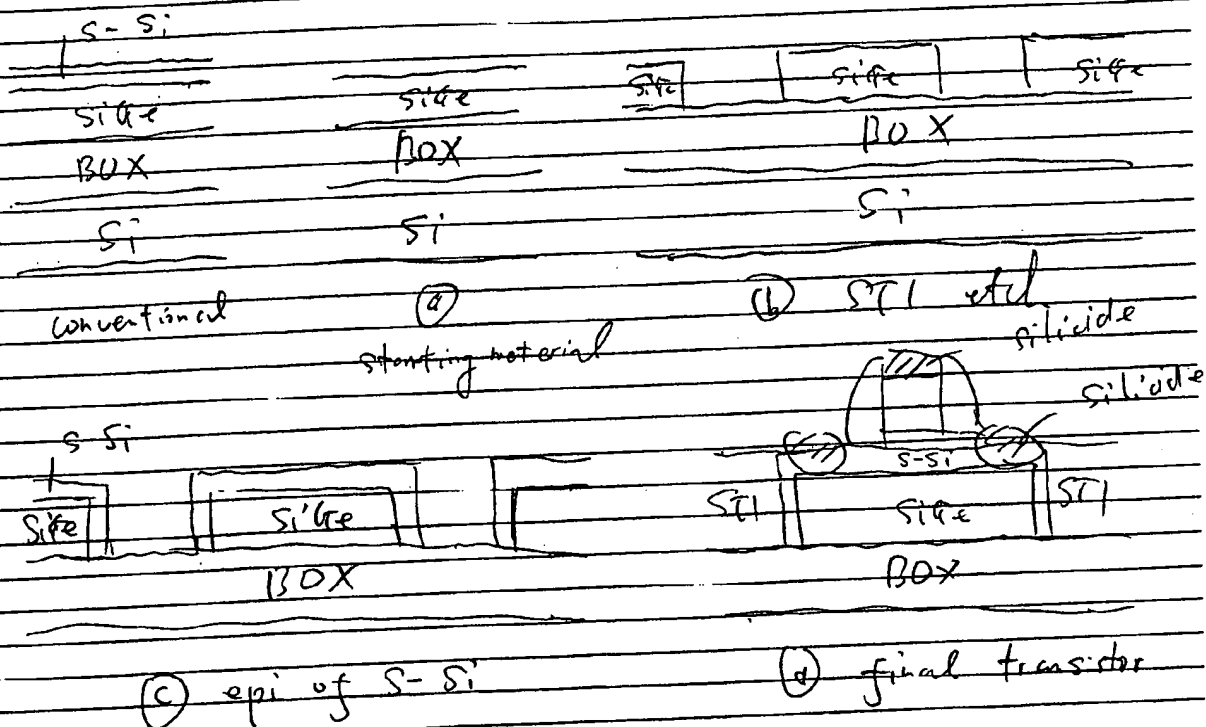
3DIP (for SSOI Harvesting) Revised 06/10/2001 **AMD CONFIDENTIAL** Attorney-Client Privileged Information Page 1



Identify known relevant art (patents, publications, other information): _____

State the problem solved by the invention: Si overhang @ STI edge, S-Si consumption before STI, STI sidewall leakage.

Brief description and sketch of the invention (please attach copies of documents like AMD patent notebook pages, reports and drawings that are helpful in describing / understanding the invention): _____



Patent notebook # _____ Page numbers _____ Number of drawings _____

Witness 1 initial: _____

Witness 2 initial: _____